

REMARKS

At the time of the Office Action dated October 12, 2006, claims 1-8 were pending in this application. In this Amendment, claims 1 and 3 have been amended, and claim 2 canceled. Care has been exercised to avoid the introduction of new matter. Support for the amendment of claim 1 can be found on, for example, page 5, line 11 to page 6, line 3 of the specification. Claim 3 has been amended to be dependent on claim 1.

Claims 1 and 3-8 are now active in this application, of which claim 1 is independent. A Request for Continued Examination is filed herewith.

Information Disclosure Statement

The Office Action dated May 3, 2006, has acknowledged the submission of the Information Disclosure Statement of April 12, 2004, and stated that the cited references have been considered. It is noted, however, that the form PTO-1449 exhibits the Examiner's initials for only two of the three references that were submitted and listed on the form, presumably an inadvertent error. Acknowledgement of consideration of the AMBA publication in a further copy of the PTO-1449 is respectfully solicited for clarification of the record.

Claim 1-8 have been rejected under 35 U.S.C. §102(b) as being anticipated by Ganapathy et al.

In the statement of the rejection, the Examiner asserted that Ganapathy et al. discloses an apparatus for distributed direct memory access for systems on chip identically corresponding to what is claimed. It is noted that the rejection of claim 2 has been rendered moot by cancellation of the claim.

Applicant submits that Ganapathy et al. does not disclose a direct memory access controller including all the limitations recited in independent claim 1. Specifically, the reference does not disclose, at a minimum, “a group of registers for next transfer which is different from said group of registers for current transfer,” recited in claim 1.

The group of registers for current transfer and the group of registers for next transfer of the claimed invention are purportedly identified as DMA descriptor registers described in paragraph [0029] of Ganapathy et al. (see paragraphs 5 and 6 of the present Office Action). It is, however, apparent that Ganapathy et al. does not disclose or suggest, at a minimum, that there are DMA descriptor registers for current transfer, and there are DMA descriptor registers for next transfer which are different from those for current transfer. In contrast, claim 1 requires a group of registers for next transfer which is different from the group of registers for current transfer in a direct memory access controller.

Accordingly, Ganapathy et al. does not identically disclose a direct memory access controller including all the limitations recited in independent claim 1 within the meaning of 35 U.S.C. §102. Dependent claims 3-8 are also patentably distinguishable over Ganapathy et al. at least because these claims respectively include all the limitations recited in independent claim 1. Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1 and 3-8, and favorable consideration thereof.

Conclusion

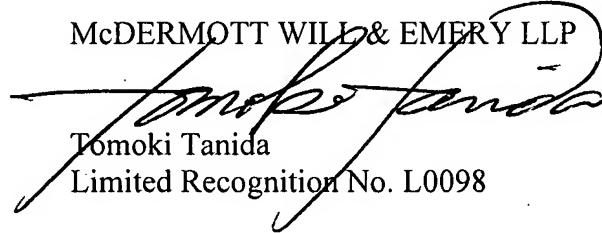
It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

Application No.: 10/821,985

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

A handwritten signature in black ink, appearing to read 'Tomoki Tanida', is written over the printed name and firm name.

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